REMARKS

Claims 1-5, 10-17, 23-25 and 29-43 have been rejected under 35 U.S.C. 103 as being unpatentable over Yojima et al. (U.S. Patent No. 6,133,744, hereinafter "Yojima"). This rejection is traversed for the following reasons.

Claim 1 has been amended to recite "a probe wafer having an auxiliary test circuit fabricated thereon". Support for this amendment is found in the specification as originally filed at paragraph [0019]. No new matter is added.

It is not clear which element of Yojima corresponds with a probe wafer as recited by Claim 1, as the Examiner's rejection does not provide any correspondence between the recited elements of Claim 1 and the elements of Yojima.

Thus, the following argument assumes that the Examiner believes that the multilayered substrate 22 of Yojima corresponds with a "probe wafer" as recited by Claim 1.

As indicated by the Examiner, Yojima does not explicitly teach that the multilayered substrate 22 includes an auxiliary test circuit. In fact, Yojima teaches the use of external LSI test chips 23, which must be mounted on an upper surface of substrate 22. (Yojima, col. 4, lines 15-18.) Such mounting would necessarily require undesirable alignment and connection steps. Yojima fails to identify the material(s) used to form multilayered substrate 22, and fails to teach that any circuitry can be fabricated on this substrate 22. For the foregoing reasons, Yojima fails to teach "a probe wafer having an auxiliary test circuit fabricated thereon" as recited by Claim 1.

In addition, Claim 1 recites "a prober configured to … place the first set of pads of the test wafer into contact

with the second set of pads of the probe wafer". (Emphasis added.)

Again, it is not clear which elements of Yojima correspond with "a prober" and "a test wafer" as recited by Claim 1, as the Examiner's rejection does not provide any correspondence between the recited elements of Claim 1 and the elements of Yojima.

Thus, the following argument assumes that the Examiner believes that the wafer 29 of Yojima corresponds with "a test wafer" as recited by Claim 1.

Yojima does not teach that the pads of the wafer 29 are placed into contact with the contacts (not shown) of multilayered substrate 22. Instead, Yojima teaches that contact film 24 is required to provide electrical connection between the contacts of substrate 22 and the pads of wafer 29.

For this reason, Yojima fails to teach "a prober configured to … place the first set of pads of the test wafer into contact with the second set of pads of the probe wafer" as recited by Claim 1.

For the foregoing reasons, Claim 1 is allowable over Yojima. Claims 2-5 and 10-17, which depend from Claim 1, are allowable over Yojima for at least the same reasons as Claim 1.

In addition, Claim 4 recites "wherein each of the dies includes a non-volatile memory array". The Examiner indicates that "Yojima teaches the testing of a DRAM semiconductor wafer". However, DRAM is not non-volatile memory. For this additional reason, Claim 4 is allowable over Yojima.

In addition, Claim 10 recites "the probe wafer further comprises a plurality of electrically conductive studs

located on the second set of pads, wherein the conductive studs contact the first set of pads on the test wafer when the probe wafer is coupled to the test wafer".

In contrast, Yojima teaches that bumps 25a are located on contact film 24, and not on substrate 22. (Yojima, Col. 4, line 66 to Col. 5, line 5; Fig. 3.) In addition, these bumps 25a do not contact the wafer 29. Rather bumps 25b on the underside of contact film 24 contact the wafer 29. Consequently, Yojima does not teach "the probe wafer further comprises a plurality of electrically conductive studs located on the second set of pads, wherein the conductive studs contact the first set of pads on the test wafer" as recited by Claim 10. For these additional reasons, Claim 10 is allowable over Yojima.

In addition, Claim 11 recites "the interconnect structure of the probe wafer extends around edges of the probe wafer". In contrast, Yojima teaches that the internal wirings 26 extend through multilayered substrate 22. (Yojima, Col. 4, lines 22-25; Fig. 2.) Consequently, Yojima fails to teach an interconnect structure that "extends around the edges of the probe wafer" as recited by Claim 11. For this additional reason, Claim 11 is allowable over Yojima.

In addition, Claim 16 recites "wherein the probe wafer comprises a monocrystalline semiconductor material". Yojima fails to teach or suggest the composition of multilayered substrate 22. Thus, Yojima fails to teach or suggest that multilayered substrate 22 includes a monocrystalline semiconductor material as recited by Claim 16. For this additional reason, Claim 16 is allowable over Yojima.

Claim 24 recites "transmitting the first set of test signals from the second set of pads to test circuitry fabricated on the probe wafer". As described above, Yojima does not teach "test circuitry fabricated on the probe wafer" as recited by Claim 24. For this reason, Claim 24 is allowable over Yojima.

Claim 25, which depends from Claim 24, is allowable over Yojima for at least the same reasons as Claim 24.

Claim 29 recites "A probe wafer comprising: a substrate" and "test circuitry fabricated on the substrate". As described above, Yojima fails to teach test circuitry fabricated on substrate 22. For this reason, Claim 29 is allowable over Yojima.

In addition, Claim 29 recites a "first set of pads having a pattern to correspond with a pattern of pads on a test wafer". In contrast, Yojima teaches that the pattern of contacts on the lower surface of multilayered substrate 22 is different than the pattern of contacts on wafer 29. (Yojima, Col. 5, lines 9-11; Fig. 3.) For this reason, Yojima fails to teach a "first set of pads having a pattern to correspond with a pattern of pads on a test wafer" as recited by Claim 29.

For these reasons, Claim 29 is allowable over Yojima. Claims 30-42, which depend from Claim 29, are allowable over Yojima for at least the same reasons as Claim 29.

In addition, Claim 30 recites "a first set of the traces extend around outer edges of the substrate". As described above in connection with Claim 11, Yojima fails to teach a first set of traces as recited by Claim 30. For this additional reason, Claim 30 is allowable over Yojima.

In addition, Claim 39 recites "the substrate comprises a monocrystalline semiconductor material". As described

above in connection with Claim 16, Yojima fails to teach or suggest the composition of multilayered substrate 22. Thus, Yojima fails to teach or suggest that multilayered substrate 22 includes a monocrystalline semiconductor material as recited by Claim 39. For this additional reason, Claim 39 is allowable over Yojima.

Claim 40, which recites "the substrate comprises silicon", and Claim 41, which recites "the substrate comprises a ceramic or glass material", are allowable over Yojima for reasons similar to Claim 39.

Claims 6-9, 18-22 and 26-28 have been objected to, presumably for being dependent upon a rejected base claim. If so, these claims would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. However, because Applicant believes that the base claims are allowable for the reasons provided above, Claims 6-9, 18-22 and 26-28 are not amended at this time.

## CONCLUSION

Claims 1-43 are pending in the present Application. Claims 6-9, 18-22 and 26-28 are allowable. Reconsideration and allowance of Claims 1-5, 10-17, 23-25 and 29-43 is respectfully requested. If there are any questions, please telephone the undersigned at (925) 895-3545 to expedite prosecution of this case.

Respectfully submitted,

Customer No. 022888

E. Eric Hoffman
Attorney for Applicant
Reg. No. 38,186

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6-15-04 Carrie Reddick

Date Signature: Carrie Reddick